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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,605	10/13/2003	Bret R. Dale	BUR920030111US1	2604
21918	7590	11/18/2005	EXAMINER	
DOWNS RACHLIN MARTIN PLLC 199 MAIN STREET P O BOX 190 BURLINGTON, VT 05402-0190			ROSSOSHEK, YELENA	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/605,605	DALE ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 9, 10, 12, 16, 17, 19 and 20 is/are rejected.
- 7) ☒ Claim(s) 4-8, 14, 15 and 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>4/26/04</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the Application 10/605,605 filed 10/13/2003.
2. Claims 1-20 are pending in the Application.

Claim Objections

3. Claims 2, 12 are objected to because of the following informalities: claims 2, 12 recite the limitation "wherein at least some of the plurality of timing paths . . .". There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2, 11-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 2, 12 Specification fails to support or describe "the step of fixing said early mode problems" before step b), which is inserting a delay element into the timing path, instead paragraph [0023] describes the step of fixing said early mode problems" by inserting a delay element.

As to claims 11, 13 Specification fails to support the limitation “. . . of removing at least one timing path from said portion of the plurality of timing paths”.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 9, 10, 12, 16, 17, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Brennan et al. (US Patent 6,434,731).

With respect to claims 1 Brennan et al. teaches a method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths within a method of automated design of a clock distribution network with minimal clock skew (col. 4, ll. 8-11), wherein the clock skew is had a dependency of the voltage level on the path (col. 2, ll.9-19), comprising the steps of: (a) determining for each one of the plurality of timing paths a corresponding delay as shown on the Figs. 4a, 4b plurality of paths (col. 6, ll.35-37), wherein the skew is determined for each path (col. 8, ll.18-20); and (b) inserting a delay element into each one of the plurality of timing paths having said corresponding delay, said delay element configured to induce said corresponding delay into that one of the plurality of timing paths using one of the techniques to reduce clock skew, such as inserting delay into clock distribution network (col. 2, ll.66-67; col. 3, ll.1-7).

With respect to claim 9 Brennan et al. teaches a method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths each having a late mode margin within a method of automated design of a clock distribution network with minimal clock skew (col. 4, ll. 8-11), wherein the clock skew is had a dependency of the voltage level on the path (col. 2, ll.9-19), comprising the steps of: (a) determining if the late mode margin of each one of the plurality of timing paths is greater than zero within determining the skew as a late mode (col. 2, ll.28-30); and (b) for each one of the plurality of timing paths having a late mode margin greater than zero, determining a delay for that one of the plurality of timing paths, said delay being a function of the corresponding late mode margin within determining a specific amount of delay for each timing path considering the difference between the various signal paths (col. 3, ll.2-8).

With respect to claim 16 Brennan et al. teaches an integrated circuit, comprising: (a) a plurality of timing paths each having a late mode margin within determining the skew as a late mode (col. 2, ll.28-30); (b) a delay element located in each one of at least some of said plurality of timing paths, each of said delay elements having a delay that is a function of said late mode margin of the corresponding one of said plurality of timing paths within determining a specific amount of delay for each timing path considering the difference between the various signal paths (col. 3, ll.2-8).

With respect to claims 2, 3, 10, 12, 17, 19, 20 Brennan et al. teaches:

Claims 2, 12: wherein at least some of the plurality of timing paths each have early mode problems (col. 2, ll.37-39), the method further comprising, prior to step (b), the step of fixing said early mode problems (col. 2, ll.60-63; col. 4, ll.3-7);

Claims 3, 10, 17 : wherein each one of the plurality of timing paths has a corresponding late mode margin and step (a) includes setting each said corresponding delay to said corresponding late mode margin (col. 4, ll.18-24);

Claim 19: wherein said plurality of timing paths each have an early mode margin and each said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths (col. 3, ll.4-7; ll.22-24);

Claim 20: wherein at least one delay is substantially equal to the difference between the late and early mode margins of the corresponding one of the plurality of timing paths minus a predetermined period col. 3, ll.4-7; ll.22-24).

Allowable Subject Matter

8. Claims 4-8, 14, 15, 18 are allowed. The prior art of record does not teach the overall instantaneous current draw has a profile and step (a) includes setting each one of at least some of said corresponding delays to said corresponding late mode margin minus a fraction of the timing cycle as claimed

Double Patenting

9. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis

Art Unit: 2825

added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

10. Claims 1-20 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-20 of copending Application No. 10/605,683. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

11. Claims 1-20 are directed to the same invention as that of claims 1-20 of commonly assigned by IBM Application No. 10/605,683. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

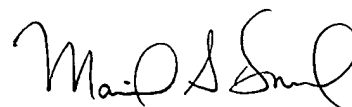
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A handwritten signature in black ink, appearing to read 'Matthew Smith', is written above the printed name.

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800